WHAT IS CLAIMED IS:

1. A method of producing a semiconductor integrated circuit device having word lines, data lines and memory cells each connected to one of the word lines and one of the data lines, said memory cells each having (1) a MISFET having a gate electrode and a source region and a drain region on a semiconductor substrate and (2) a capacitor element connected in series, comprising the steps of:

(a) forming a first electrode for said capacitor element over said gate electrode of said MISFET, said first electrode being electrically connected to one of said source region and drain region and extending over said gate electrode;

(b) depositing a dielectric film on said first electrode;

(c) depositing a conductive film on said dielectric film;

(d) forming a mask layer having a predetermined pattern larger than said first electrode in directions which said data lines and said word lines extend, over said conductive film, and

(e) etching both said conductive film and said dielectric film at a portion exposed from said mask layer in order to form a second electrode for said capacitor element, wherein said etching also etches said dielectric film over the other of the source and drain regions of the MISFET.

2. A method of producing a semiconductor integrated circuit device according to claim 1, wherein after said etching, said dielectric film exists only under said second electrode.

3. A method of producing a semiconductor integrated circuit device according to claim 1, wherein said dielectric film has at least a double-layer structure of a silicon nitride film and a silicon oxide film stacked on the silicon nitride film.

4. A method of producing a semiconductor integrated circuit device having MISFETs arranged in a first direction and in a second direction which is perpendicular to said first direction, each of said MISFETs having a gate electrode and a source region and a drain region, and capacitor elements each having a first electrode respectively connected to one of the source region and the drain region of a respective one of said MISFETs, a dielectric film and a second electrode, comprising the steps of:

(a) depositing a first conductive film over a semiconductor substrate;

(b) patterning said first conductive film in order to form first electrodes for said capacitor elements, said first electrodes being arranged in said first and

second directions, each first electrode extending respectively over gate electrodes of said MISFETs;

(c) depositing a dielectric film on said first electrode;

(d) depositing a second conductive film on said dielectric film; and

(e) etching said second conductive film and said dielectric film in order to form a second electrode for said capacitor element and a patterned dielectric film, wherein said patterned dielectric film has substantially a same pattern as that of the second electrode and exists only under said second electrode, said patterned dielectric film not extending over the other of the source region and the drain region of the respective one of the MISFETs, and wherein said second electrode is larger than said first electrode in said first and second directions.

5. A method of producing a semiconductor integrated circuit device having MISFETs arranged in a first direction and in a second direction which is perpendicular to said first direction, each of said MISFETs having a gate electrode and a source region and a drain region, and capacitor elements each having a first electrode respectively connected to one of the source region and the drain region of a respective one of said MISFETs, a dielectric film and a second electrode, comprising the steps of:

(a) forming the first electrode for the capacitor element over a semiconductor substrate, each first electrode extending respectively over gate electrodes of said MISFETs;

(b) depositing a dielectric film on said first electrode;

(c) depositing a conductive film on said dielectric film; and

(d) patterning said conductive film and said dielectric film respectively to form a second electrode and a patterned dielectric film, wherein said patterned dielectric film has substantially a same pattern as that of said second electrode, said patterned dielectric film not extending over the other of the source region and the drain region of the respective one of the MISFETs, and wherein said second electrode is larger than said first electrode in said first and second directions.

6. A method of producing a semiconductor integrated circuit device according to claim 5, wherein said second electrode covers both said insulating film and a respective first electrode.

7. A method of producing a semiconductor integrated circuit device according to claim 5, wherein said second electrode covers a respective first electrode.